CLAIMS

1. An integrated circuit graphics controller system for connection to a CPU and a display, said controller system comprising

a graphics engine for manipulating video data responsive to instructions from said CPU;

a video memory holding said video data; and

a data interface between said graphics engine and said video memory, said interface being at least 64 bits wide;

whereby said graphics controller system reduces power dissipation.

2. The graphics controller system of claim 1 further comprising a PCMCIA host adaptor.

3. The graphics controller system of claim 1 further comprising an infrared interface.

4. The graphics controller system of claim 1 wherein said memory has a size intermediate 218 x 8 x n bits, where n is an integer.

5. The graphics controller system of claim 4 wherein said memory is 218 X 28 bits.

6. The graphics controller system of claim 5 wherein said data interface is 128 bits wide.

7. An integrated circuit graphics controller system for connection to a CPU and a display, said controller system comprising

a graphics engine for manipulating video data responsive to instructions from said CPU, said graphics engine having logic circuits formed from P-channel and N-channel transistors, said P-channel transistors having sources connected to a first voltage supply line, said N-channel transistors having sources connected to a second voltage supply line, and said N-channel transistors placed in a substrate region connected to a third voltage supply line, said third voltage supply lower than said second voltage supply;

a video memory holding said video data; and

a data interface between said graphics engine and said video memory;

whereby said graphics controller system reduces power dissipation.

8. The integrated circuit graphics controller system of claim 7 wherein said video memory has a capacity of at least 2 megabits, and said graphics controller comprises at least 30K logic gates.

9. An integrated circuit graphics controller system for connection to a CPU and a display, said controller system comprising

a graphics engine for manipulating video data responsive to instructions from said CPU, said graphics engine having analog circuits comprising mostly P-channel transistors; a video memory holding said video data; and

a data interface between said graphics engine and said video memory;

whereby said graphics controller system reduces power dissipation.

10. An integrated circuit comprising

a logic portion having at least 30K logic gates; and

a memory portion having a capacity of at least 2 megabits.

11. The integrated circuit of claim 10 wherein said logic gates have P-channel and N-channel transistors, said P-channel transistors having sources connected to a first voltage supply line, said N-channel transistors having sources connected to a second voltage supply line, and said N-channel transistors placed in a substrate region connected to a third voltage supply line, said third voltage supply lower than said second voltage supply.